Loss-Compensated Distributed Baseband Amplifier IC's for Optical Transmission Systems

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***Abstract*—We describe a distributed baseband amplifier using a new loss compensation technique for the drain artificial line. The new loss compensation circuit improves a high-frequency performance of the amplifier and makes the gain bandwidth product of the amplifier larger than that of conventional ones. We also use dc matching terminations and dumping resistors for the gate and drain artificial lines to obtain flat gain from frequencies as low as 0 Hz. One IC fabricated using 0.1 μm-gate-length InAlAs/InGaAs/InP HEMT's has a gain of 16 dB over a 0-to-50 GHz band, resulting in a gain bandwidth product of about 300 GHz. Another IC has a gain of 10 dB over a 0-to-90 GHz band. These are the highest gain bandwidth product and the widest band reported for baseband amplifier IC's applicable to optical transmission systems.**

I. Introduction

IN FUTURE high-speed optical transmission systems, the equalizing amplifier will be one of the most important components. According to the synchronous digital hierarchy (SDH) standard, the transfer section overhead should be inserted in the data bit stream every 125 μs. This corresponds to a frequency of 8 kHz and determines the lower limit of the frequency of the amplifier [1]. As a consequence, the baseband amplifiers in current systems have been designed as dc amplifiers using only lumped elements, which makes it easy to achieve a high gain over a frequency range starting from 0 Hz. The upper limit on frequency, however, is restricted by the parasitic capacitances (R-C cut-off frequency) of transistors. It is thus very difficult to attain a millimeter-wave bandwidth with conventional lumped-circuit design techniques.

Distributed amplifiers, on the other hand, have been investigated for use in microwave and millimeter-wave bands. They have input and output artificial lines made up of a series of transmission lines (L_g and L_d in Fig. 1) and the parasitic capacitances (C_{gs} and C_{ds} in Fig. 1) of transistors. Because these artificial lines have a very high L-C cut-off frequency, the amplifiers inherently have wideband characteristics. The distributed amplifying technique is therefore the best way to build baseband amplifiers that will meet the requirements of tomorrow's transmission systems. Conventional distributed amplifiers, however, cannot achieve these potentially wideband characteristics because the losses in the artificial lines are large at high frequencies [2]. Moreover, almost all of them are unable to operate from frequencies as low as 0 Hz.

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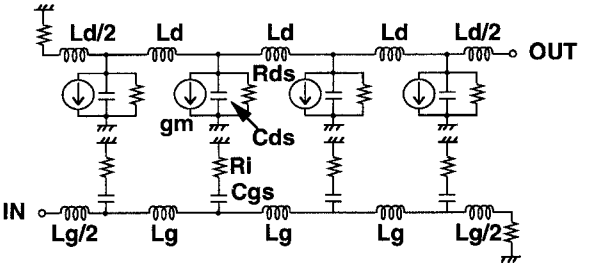

Fig. 1. Equivalent circuit of a conventional common-source distributed amplifier.

We therefore propose new techniques for loss compensation and dc termination. The proposed loss compensation circuit improves the high-frequency performance of the amplifier, and the dc terminations with dumping resistors make the gain flat from 0 Hz and reduces the effect of the parasitic impedance at the bias terminal.

II. Design Principle

A. Gain Degradation of the 3dB Bandwidth by the Lossy Artificial Lines

The gate and drain artificial lines of a distributed amplifier have high-frequency losses caused by the resistances (R_i and R_{ds} in Fig. 1) of the transistors. Therefore, the gain tends to decrease at high frequencies and the 3-dB bandwidth narrows remarkably below the cut-off frequency of the gate and drain artificial lines. The per-section attenuation constants of a conventional single-common-source distributed amplifier are approximated as

$$\alpha_g = \frac{X_g^2 \cdot K_g}{\sqrt{1 - X_g^2(1 - K_g^2)}} \tag{1}$$

and

$$\alpha_d = \frac{1}{K_d\sqrt{1 - X_d^2}} \tag{2}$$

where

$$X_g = \frac{\omega}{\omega_{cg}}, K_g = \frac{\omega_{cg}}{\omega_g}$$

$$X_d = \frac{\omega}{\omega_{cd}}, K_d = \frac{\omega_{cd}}{\omega_d}$$

$$\omega_{cg} = \frac{2}{\sqrt{L_g \cdot C_{gs}}}, \omega_{cd} = \frac{2}{\sqrt{L_d \cdot C_{ds}}}$$

$$\omega_g = \frac{1}{R_i \cdot C_{gs}}, \omega_d = \frac{1}{R_{ds} \cdot C_{ds}}.$$

Here L_g and L_d are the per-section inductances of the gate and drain line.

If we compare the attenuation constants, $N \cdot \alpha_{g(\omega)}$ and $N \cdot \alpha_{d(\omega)}$ (where N is the number of sections), of two distributed amplifiers that have the same total gate width but different configurations (for example, one has three 50-μm sections and the other has six 25-μm sections), those of the narrow-per-section-gate-width (w_g) amplifier are lower than those of the wide-w_g amplifier at the same ω. The cut-off frequency of the narrow-w_g amplifier is also higher than that of the wide-w_g amplifier. Thus we can improve the 3-dB bandwidth of the distributed amplifier by using sections with narrow gates. But if we compare the attenuation constants, $N \cdot \alpha_g$ as functions of frequency normalized by the gate-line cut-off frequency of each amplifier (X_g), the $N \cdot \alpha_{g(X_g)}$ of the narrow-w_g amplifier is higher than that of the wide-w_g amplifier at the same X_g (not at the same ω) [2]. As functions of X_d, on the other hand, the $N \cdot \alpha_{d(X_d)}$ values of both amplifiers are the same. This means that the ratio of the 3-dB bandwidth to the cut-off frequency is decreased when we distribute the gate width. Eventually, the improvement of the 3-dB bandwidth is saturates as this gate-line loss increases.

Gate-line-loss compensation is thus crucial to improving the gain bandwidth product (GBWP) of distributed amplifiers. One of the effective ways to increase this product is by constructing a capacitive-division distributed amplifier [3–4]. Additional series capacitances at the gate terminal decrease the values of the shunt capacitance of the gate line and reduce the high-frequency loss. The gain of the amplifier decreases, however, because the input signal voltage amplitude is divided by the additional capacitance. Besides, this kind of amplifier cannot operate from 0 Hz and cannot be used as a baseband amplifier in an SDH transmission system.

As mentioned above, the improvement of the GBWP resulting from the distribution of the gate width is limited by the gate line loss. Under the existing circumstances, we cannot use even a several-micrometer gate width because the per-section transmission lines become too short to be laid out. In designing feasible IC's, we have to use a gate width of several tens of micrometers, and we therefore have to compensate the drain-line loss that predominates in amplifiers constructed of sections using transistors with wide gates.

Cascode pairs of transistors are being used to decrease this drain attenuation constant because they have a negative output shunt resistance [5]. The output impedance of the cascode pair shown in Fig. 2(a) can be written as

$$Z_{out} = \frac{Z_{ds1}}{Z_{ds1} + Z_{gs2}} \left(\frac{g_m \cdot Z_{ds2}}{j\omega C_{gs2}} + Z_{gs2} \right) + Z_{ds2} \quad (3)$$

where Z_{gs} and Z_{ds} are the gate-to-source and drain-to-source impedances of the transistor. We assume that C_{dg} is small enough to neglect. Subscripts 1 and 2, respectively, indicate the common-source and common-gate transistors. Generally speaking, C_{gs} is larger than C_{ds} under the usual bias conditions. Hence, at high frequencies (where $Mag(Z_{ds}) \gg Mag(Z_{gs})$), we can substitute unity for the first coefficient in (3). Consequently, the real part of the output impedance

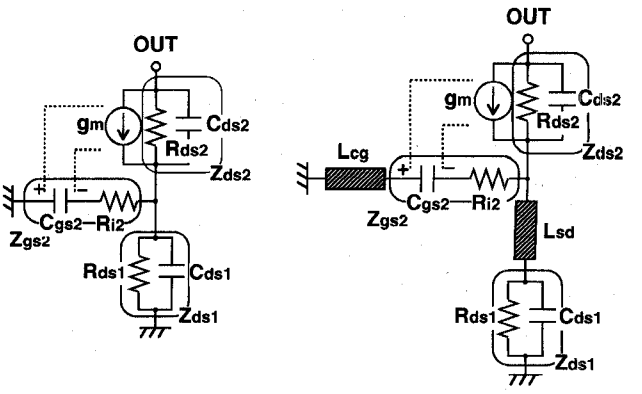

Fig. 2. Equivalent circuits of (a) a cascode pair of transistors and (b) the proposed loss compensation circuit.

can be written as

$$Re(Z_{out}) = \frac{R_{ds2}}{1 + \omega^2 C_{ds2}^2 R_{ds2}^2} \left(1 - \frac{gm_2 \cdot R_{ds2} C_{ds2}}{C_{gs2}}\right). \quad (4)$$

On the other hand, the real part of the output impedance of the single common-source transistor is written as

$$Re(Z_{out}) = \frac{R_{ds}}{1 + \omega^2 C_{ds}^2 R_{ds}^2} \quad (5)$$

which is the first term in (4). It is clear that the second term operates as negative resistance and it decreases the real part of the output impedance that causes the loss of the drain artificial line. However, this negative resistance effect cannot be controlled by circuit design techniques because it depends only on the parameters of the transistors. And if we use transistors whose C_{gs} and C_{ds} values are close, we cannot substitute unity for the first coefficient in (3). This reduction of the first coefficient weakens the loss compensation effect of the conventional cascode pair.

B. New Loss Compensation Technique

A key feature in the design of our distributed baseband amplifier, which is shown schematically in Fig. 3, is the use of a new loss compensation circuit constructed with a cascode pair of transistors and two additional transmission lines, L_{cg} and L_{sd}. The equivalent circuit is shown in Fig. 2(b). The output impedance is

$$Z_{out} = \frac{(Z_{ds1} + j\omega L_{sd})}{(Z_{ds1} + j\omega L_{sd}) + (Z_{gs2} + j\omega L_{cg})} \times \left(\frac{g_m \cdot Z_{ds2}}{j\omega C_{gs2}} + (Z_{gs2} + j\omega L_{cg}) \right) + Z_{ds2}. \quad (6)$$

Because L_{cg} cancels the Z_{gs2} in the denominator, the negative resistance increases and gain is improved at high frequencies. Consequently, we can increase the number of sections and achieve higher gain while keeping the bandwidth large. Stability, however, is lost when the real part of Z_{out} becomes negative. Fig. 4 clearly shows this effect. If the value (or length) of L_{cg} is increased, S_{21} and S_{22} increase at high frequencies and the amplifier becomes unstable. S_{21} and S_{22} have peaks near the cut-off frequency and S_{22} exceeds 0 dB.

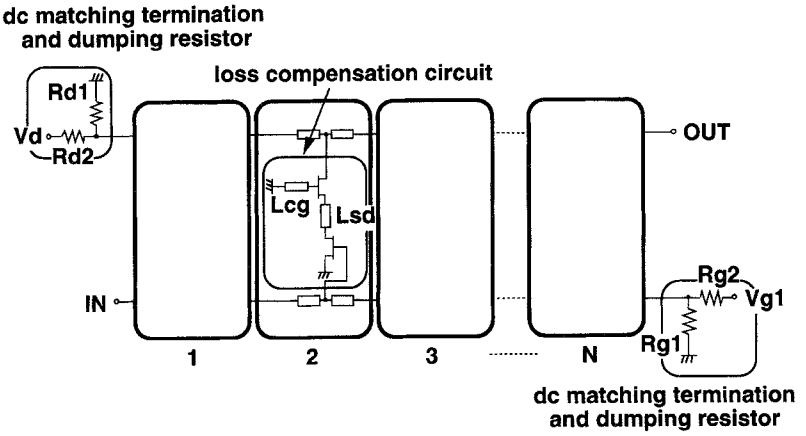

Fig. 3. Schematic circuit of the proposed loss-compensated distributed baseband amplifier.

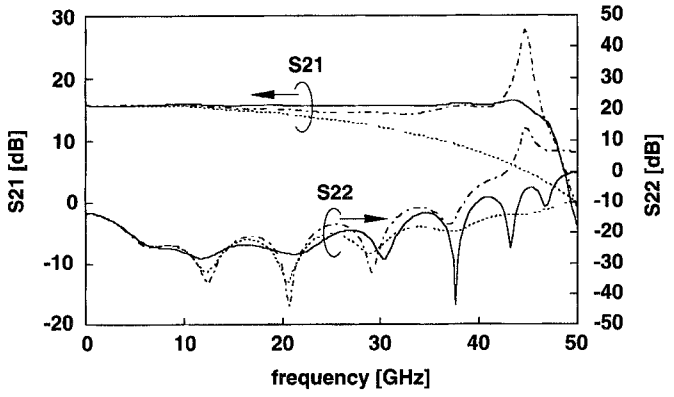

Fig. 4. The effect of the addition of L_{cg} and L_{sd}. Solid line: Loss-compensated amplifier (with L_{cg} and L_{sd}). Dotted line: Conventional cascode amplifier. Chain line: Loss-compensated amplifier with only L_{cg}.

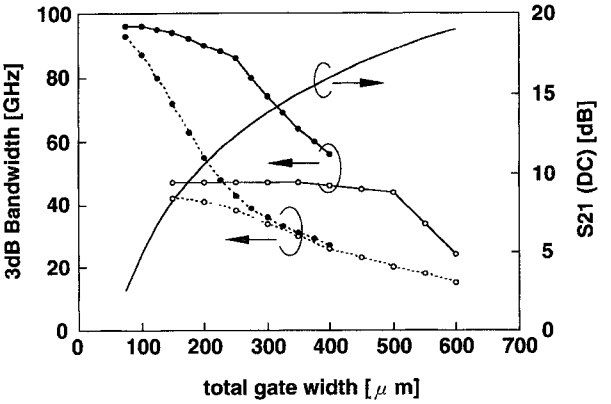

Fig. 5. Simulated dc gain and 3-dB bandwidth versus total gate width for proposed and conventional distributed baseband amplifiers. Solid line with open circles: Proposed loss-compensated amplifier (w_g = 50 μm). Solid line with closed circles: Proposed loss-compensated amplifier (w_g = 25 μm). Dotted line with open circles: Conventional cascode amplifier (w_g = 50 μm). Dotted line with closed circles: Conventional cascode amplifier (w_g = 25 μm). Solid line: DC gain.

The effect of the other transmission line (L_{sd}) is also shown in Fig. 4. From (6), we can see that L_{sd} cancels out the Z_{ds1} on the first coefficient. This can reduce the effect of L_{cg} and change the frequency dependence of the negative resistance term. If the value (or length) of L_{sd} increases, the stability of the amplifier is restored and we can obtain a flatter response than that designed without L_{sd}.

The simulated dc gain and 3-dB bandwidth are shown in Fig. 5 as a function of total w_g both for the proposed amplifier and for the conventional cascode amplifier. In this simulation, we used the derived-M type filter configurations for the drain artificial line of the conventional amplifier. It is clear that the 3-dB bandwidths of the proposed circuit are greater than those of the conventional amplifier. The configuration giving the best GBWP is one with twelve 25-μm sections (w_g =300 μm, which is twice that of conventional amplifier) and results in a simulated GBWP of 362 GHz (Fig. 6). This GBWP is greater than that of the conventional amplifier (188 GHz) by 93 percent with transistors having 25-μm-wide gates. If we use transistors with 50-μm-wide gates, the best GBWP we can achieve with the proposed circuit is 337 GHz. That of the conventional amplifier, on the other hand, is only 168 GHz, or about half as high. Because our proposed circuit compensates for the drain line loss, it is effective for amplifiers using transistors with wide gates.

C. DC Matching Terminations and Dumping Resistors

Almost all of the distributed amplifiers reported so far can not operate from frequencies as low as 0 Hz. Some of them have no dc matching termination to reduce their power dissipation. Our idea is to use the dc matching terminations R_{g1} and R_{d1} to achieve a flat gain from 0 Hz (Fig. 3). The value of R_{g1} is almost the same as the matching impedance, but R_{d1} is higher in order to compensate for output impedance reduction at low frequencies, which is caused by the output impedances of the cascode pairs connected in parallel with the drain termination.

Moreover, we use dumping resistors R_{g2} and R_{d2} to reduce the parasitic effects of external inductances at the bias terminals. These inductances usually make ripples in the frequency response of the amplifier. If we use large on-chip capacitors with a small dumping resistor to short the rf signals at the bias terminals, resonances between the capacitors and the inductances cause peaks and dips in the frequency responses at low frequencies. At the drain bias terminal, however, we cannot use a large dumping resistor because the bias voltage becomes very high. To reduce the drain bias voltage, we made

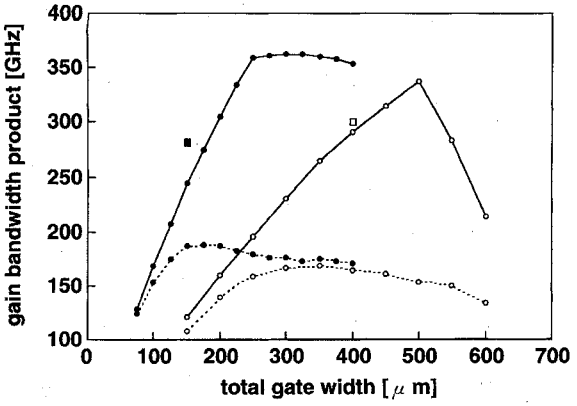

Fig. 6. Comparisons between the simulated and measured gain bandwidth products of the distributed baseband amplifiers. Solid line with open circles: Simulated GBWP of loss-compensated amplifier ($w_g = 50$ μm). Solid line with closed circles: Simulated GBWP of loss-compensated amplifier ($w_g = 25$ μm). Dotted line with open circles: Simulated GBWP of conventional cascode amplifier ($w_g = 50$ μm). Dotted line with closed circles: Simulated GBWP of conventional cascode amplifier ($w_g = 25$ μm). Open square: Measured GBWP of the IC (eight 50-μm sections). Closed square: Measured GBWP of the IC (six 25-μm sections).

the value of R_{d2} as small as possible and made the total parallel resistance of R_{d1} and R_{d2} higher than the matching impedance.

III. Fabrication

We fabricated loss-compensated distributed baseband amplifier IC's with two kinds of configurations. One, consisting of eight 50-μm sections, is the largest configuration limited by the chip size. Using transistors with 50-μm-wide gates decreases the number of sections and reduces a parasitic effect caused by the small pieces of ground patterns which are divided by the input and output coplanar waveguides. To compare the proposed amplifier with our previously reported one [1] we made another amplifier with six 25-μm sections, which is the best configuration for the conventional amplifier. The circuits of these IC's are shown in Fig. 7. We used the self-bias circuit for the common-gate terminal of each cascode pair of transistors in the amplifier with six 25-μm sections. These reduce the parasitic effect caused by the bias line of the common-gate terminal that divides the ground patterns and goes across the signal lines.

MMIC's were fabricated using our 0.1-μm gate-length InAlAs/InGaAs/InP HEMT's [6]. The HEMT's have T-shaped gates and a multifinger gate pattern. One feature of this transistor is its nonalloyed ohmic contact for drain and source electrodes. We used an n^+-InGaAs/n^+-InAlAs cap layer to reduce the contact resistance so we could make the source resistance low. The HEMT's in a 2-inch wafer have an average f_T of 140 GHz and f_{max} of 180 GHz. Moreover, we used coplanar waveguide technology in making the transmission lines. Microphotographs of the amplifiers are shown in Fig. 8. Chip sizes are 1.5×4.0 mm and 1.0×2.0 mm.

IV. Circuit Performance

A. Scattering Parameters and Group Delay

We measured the frequency response using on-wafer rf probes and a network analyzer. We used V-band and W-band

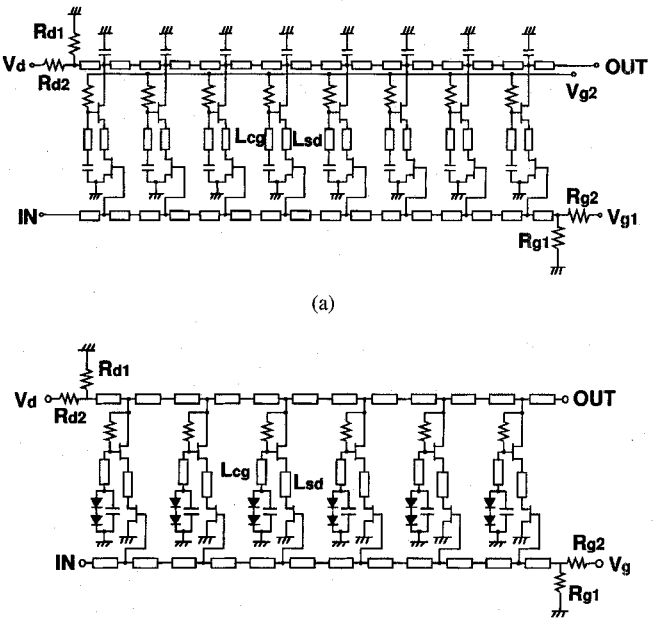

Fig. 7. Schematic circuits of the proposed loss-compensated distributed baseband amplifier IC's. (a) Eight 50-μm sections. (b) Six 25-μm sections.

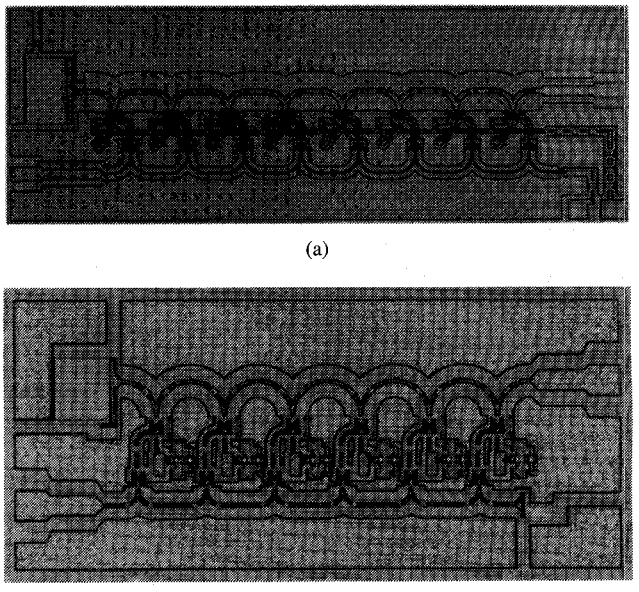

Fig. 8. Microphotographs of the loss-compensated distributed baseband amplifier IC's (a) Eight 50-μm sections. (b) Six 25-μm sections.

test sets and waveguide-input wafer probes for measurements at frequencies over 50 GHz. The measured scattering parameters are shown in Fig. 9. The amplifier IC consisting of eight 50-μm sections had a maximum gain of 16.1 dB and a 3-dB bandwidth of 47 GHz, for a GBWP of 297 GHz. The S_{11} and S_{22} values were, respectively, less than -7.9 dB (at 40.0 GHz) and less than -8.1 dB (at 38.3 GHz) below 40 GHz. Power dissipation was 1.1 W. The highest reported GBWP is 340 GHz, which was achieved with a distributed amplifier using the capacitive-division technique, but the lower limit frequency for that amplifier was 1 GHz [3]. The GBWP of our amplifier

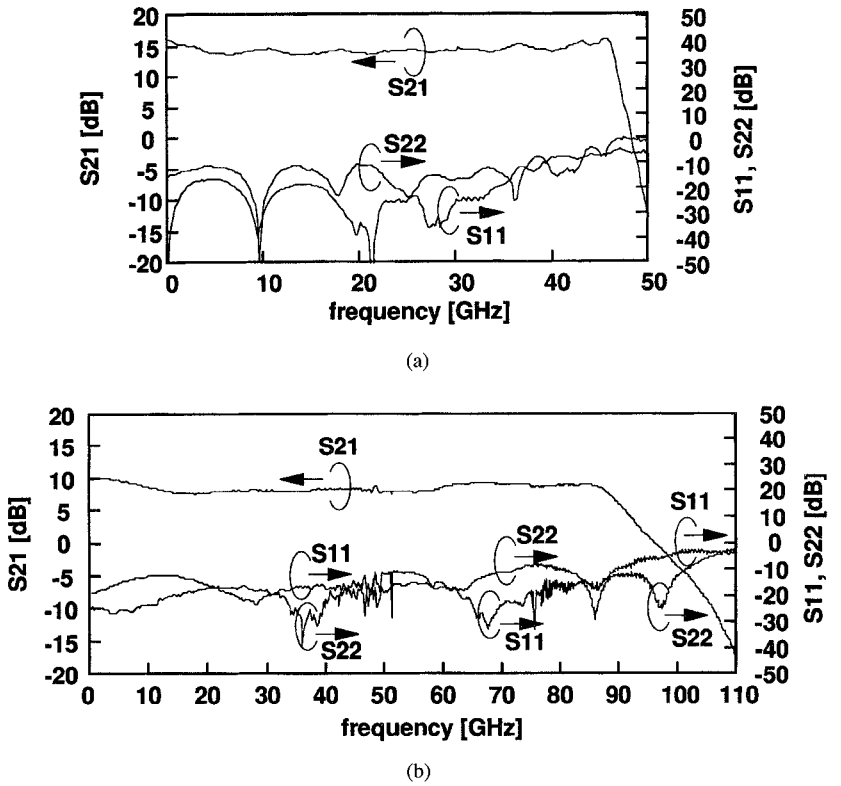

Fig. 9. Measured S parameters of the loss-compensated distributed baseband amplifier IC's. (a) Eight 50-μm sections. (b) Six 25-μm sections.

is thus the highest ever for a baseband amplifier (dc amplifier) applicable to SDH transmission systems.

The amplifier IC consisting of six 25-μm sections had a gain of 10 dB and a bandwidth of 89.2 GHz, for a GBWP of 282 GHz. The S_{11} and S_{22} values were, respectively, less than -10.6 dB (at 89.2 GHz) and less than -8.0 dB (at 76.4 GHz). Power dissipation was 860 mW. The greatest previously reported bandwidth was 5-to-100 GHz [7]. But because that amplifier also could not be used in baseband applications, the bandwidth of our amplifier is the largest yet reported for a baseband amplifier. These results are plotted in the Fig. 6, where the GBWP's calculated from measured data are in good agreement with the simulation results.

We calculated the group delay characteristics of these amplifiers from the measured S_{21} as shown in Fig. 10. The amplifier with eight 50-μm sections had a flat response of the group delay of about 60 ps in the 3-dB bandwidth, and the amplifier with six 25-μm sections also had a flat response of about 30 ps.

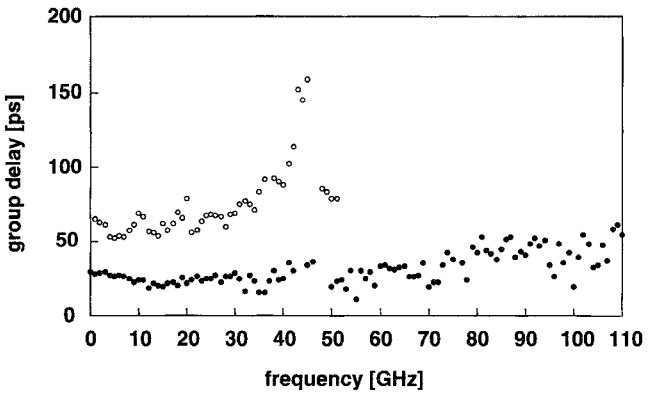

Fig. 10. Measured group delay of S_{21} of the loss-compensated distributed baseband amplifier IC's. Open circles: Eight 50-μm sections. Closed circles: Six 25-μm sections.

B. Noise Performance

We also examined the noise performance of the IC's in the frequency range of 0.5–40 GHz. The measured noise figures are shown in Fig. 11. The average noise figure of the amplifier IC with eight 50-μm sections was 5.0 dB when the amplifier was biased for maximum gain. That of the amplifier IC with six 25-μm sections was 6.5 dB.

V. Conclusion

We have developed an advanced design technique that significantly improves the performance of distributed baseband amplifier IC's. The key feature of the design is the use of a new loss-compensation circuit to improve high-frequency performance. This circuit optimizes the negative resistance in the output impedance of the cascode pair of transistors and decreases the drain line loss. In our simulation, the new loss-compensated distributed amplifier has a gain bandwidth product twice as large as that of conventional cascode ones. We also use dc matching terminations and dumping resistors to obtain a flat gain over a frequency range starting from 0 Hz.

Two kinds of distributed baseband amplifiers were fabricated using these new techniques and InAlAs/InGaAs/InP HEMT's. One amplifier IC has a flat gain of 16 dB with a 0-to-47-GHz bandwidth, for a gain bandwidth product of 297 GHz. To our knowledge, this is the highest gain bandwidth product

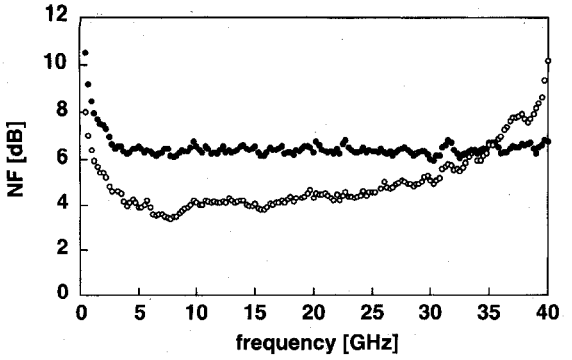

Fig. 11. Fig. 11 Measured noise figure of the loss-compensated distributed baseband amplifier IC's. Open circles: Eight 50-μm sections. Closed circles: Six 25-μm sections.

reported for a baseband amplifier IC. The other amplifier IC has a flat gain of 10 dB with a 0-to-89-GHz band, the largest bandwidth yet reported for a baseband amplifier IC. The flat group delay responses are 60 and 30 ps and the noise figures are 5.0 and 6.5 dB.

The performances of these IC's make them promising for use as preamplifiers and postamplifiers in optical receiver systems operating at more than 40 Gbit/s. We think our new techniques will break through the speed limitation of optical transmission systems.

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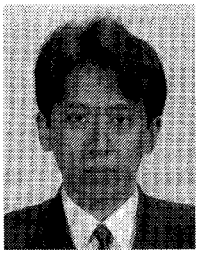

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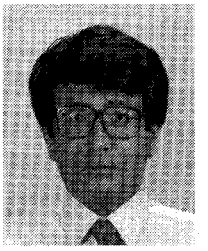

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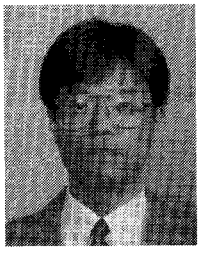

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